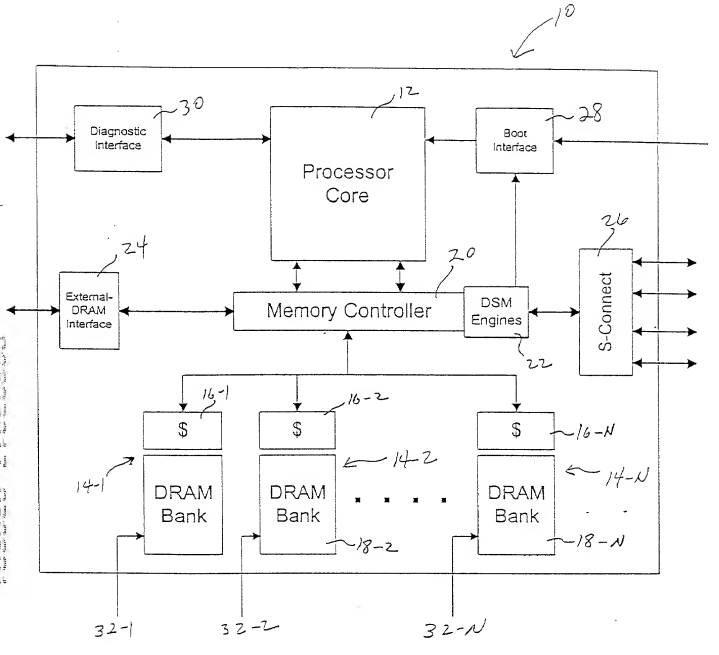
10
Diagnostic Interface
30
Processor Core
12
Boot Interface
28
External-DRAM Interface
24
Memory Controller
20
DSM Engines
22
S-Connect
26
16-1
16-2
16-N
$
$
$
14-1
14-2
14-N
DRAM Bank
DRAM Bank
DRAM Bank
18-2
18-N
32-1
32-2
32-N

Fig. 1

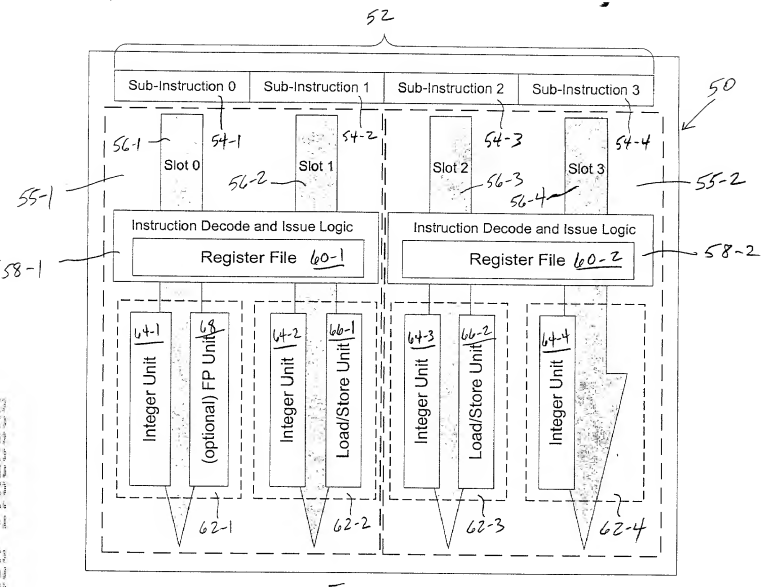
52
Sub-Instruction 0
Sub-Instruction 1
Sub-Instruction 2
Sub-Instruction 3
50
56-1
54-1
54-2
54-3
54-4
Slot 0
Slot 1
Slot 2
Slot 3
55-1
56-2
56-3
56-4
55-2
Instruction Decode and Issue Logic
Instruction Decode and Issue Logic
58-1
Register File 60-1
Register File 60-2
58-2
64-1
68
64-2
60-1
64-3
66-2
64-4
Integer Unit
(optional) FP Unit
Integer Unit
Load/Store Unit
Integer Unit
Load/Store Unit
Integer Unit
62-1
62-2
62-3
62-4

Fig. 2

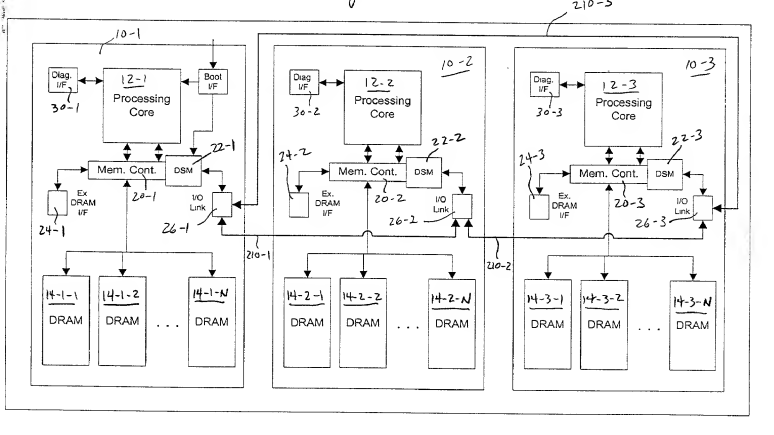
210-3
10-1
10-2
10-3
Diag. I/F
12-1
Processing Core
Bool I/F
30-1
30-2
12-2
30-3
12-3
22-1
22-2
22-3
Mem. Cont.
DSM
20-1
20-2
20-3
Ex. DRAM I/F
I/O Link
24-1
24-2
24-3
26-1
26-2
26-3
210-1
210-2
14-1-1
14-1-2
14-1-N
14-2-1
14-2-2
14-2-N
14-3-1
14-3-2
14-3-N
DRAM

Fig. 5

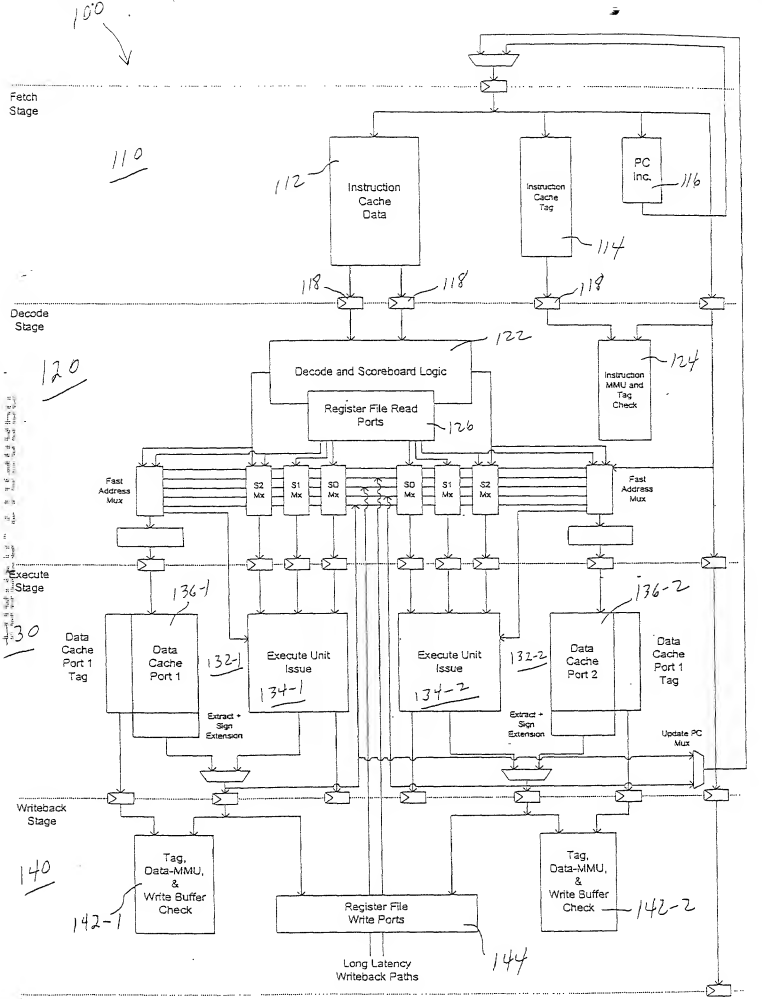
100
Fetch Stage
110
112
Instruction Cache Data
Instruction Cache Tag
114
PC Inc.
116
118
118
118
Decode Stage
120
122
Decode and Scoreboard Logic
124
Instruction MMU and Tag Check
Register File Read Ports
126
Fast Address Mux
S2 Mx
S1 Mx
S0 Mx
S0 Mx
S1 Mx
S2 Mx
Fast Address Mux
Execute Stage
130
136-1
136-2
Data Cache Port 1 Tag
Data Cache Port 1
132-1
Execute Unit Issue
134-1
Execute Unit Issue
132-2
Data Cache Port 2
Data Cache Port 1 Tag
Extract + Sign Extension
Extract + Sign Extension
Update PC Mux
Writeback Stage
140
Tag, Data-MMU, & Write Buffer Check
142-1
Register File Write Ports
144
Tag, Data-MMU, & Write Buffer Check
142-2
Long Latency Writeback Paths
Trap Stage
150

Fig. 3

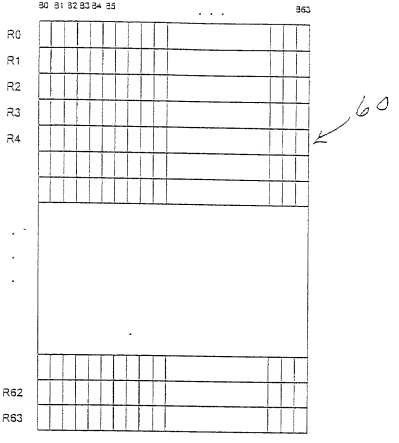

Fig. 4